Chapter 11

Design and Control of a Multilevel Inverter for Electric Vehicles Using a Single DC Source

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ABSTRACT

AC motors are predominantly used in electric vehicles (EVs) due to their high efficiency and the ability to provide more power with smaller and lighter engines. Additionally, most applications, especially EVs, require a single DC source for ease of use. In this thesis, a new 31-level multi-level inverter (MLI) circuit fed from a single source is proposed for EVs. In the proposed topology, switched diode structure is used as the main circuit and DC bus voltages are obtained by scaling asymmetrically and using high frequency link (HFL) method with toroid transformer. Nearest level control (NLC) is used for minimum total harmonic distortion (THD) in the output waveform. The simulation of the proposed topology was carried out in the Matlab/Simulink program and the simulation results were confirmed by experimental studies using FPGA. In studies, as a load; pure resistive and induction motor are used. In addition, the filter effect is shown by adding various filters to the proposed EMI. As a result, the proposed topology created a high voltage output stage with low voltage switches. A topology suitable for the EV drive system, with a single DC source and an output voltage THD value of 2.7% without using a filter, was obtained.

Keywords: Multilevel inverter, Electric vehicle driver, FPGA, HFL, High frequency link

INTRODUCTION

Today, electric vehicles (EV) are increasingly preferred in order to reduce environmental impacts and increase energy efficiency. Electric motors, an important component of EVs, are a critical element that affects vehicle performance and energy efficiency. In this context, the design and selection of the motors used in EV are of great importance (Hashemnia and Asaei, 2008). AC motors offer many advantages such as using energy in the EV as efficiently as possible, having high efficiency, high power density, reducing the weight while increasing the performance of the EV due to the fact that more power can be provided with smaller and lighter motors.

Inverters are power electronics circuits that convert DC power to AC power at the desired output frequency and voltage and are widely used in the industry. The output voltage waveform changes depending on the DC source used at the input and the number of controlled and uncontrolled power elements. The output voltage has a stepped waveform and depending on the number of levels, the THD of the voltage signal decreases and accordingly the efficiency increases.

Most of the EVs produced recently are using three phase inverters designed using IGBT due to high efficiency and low cost. The battery pack can be connected directly to the DC input of an inverter or by using a controlled DC/DC power converter. To create a three-phase sinusoidal output current to the motor, six switches are required in the motor driver circuit (Reimers et al., 2019). This inverter is called classical inverter. Conventional inverter causes switching losses to increase at high switching frequency required for high power and voltage applications. These inverters have high THD, high electromagnetic interference (EMI) and high voltage change ratio (dv/dt) (Krishna and Suresh, 2016). For high power and high voltage applications, they have the important limitation that they require the use of power electronic devices that can operate at high power and voltage. The voltage level also increases with increasing power levels for satisfactory performance in devices. A solution to the disadvantages of the classical inverter and the high voltage requirement is to cascade inverter structures (Hosseinzadeh et al., 2021). For this purpose, MLI's have been developed.

MLI topology concept was introduced in early 1975 with three-level inverters. Basically, there are three different types: Diode Clamped MLI, Capacitor Clamped MLI (Flying Capacitor) and Cascade H-bridge MLI (Hatas et al., 2023). These MLIs have advantages over conventional inverters such as reduced THD, low dv/dt, reduced switching losses and high-power quality. In addition, by operating in both fundamental and high frequency PWM, an

inverter output voltage closer to a pure sine waveform is obtained (Koshti and Rao, 2017). Flying Capacitor and Diode Clamped MLIs have a significant disadvantage due to unstable DC bus conditions and the need for high-capacity capacitors. These disadvantages can be overcome by using cascade connections of Cascade H-bridge MLI, but require a large number of switching elements for higher levels. For this reason, researchers are trying to create more useful hybrid topologies by using the advantages of traditional topologies (Ponraj et al., 2021).

MLI topologies require multiple isolated DC bus voltages. DC sources can be designed insulated in battery packs. However, additional measures are required to ensure the correct proportion of battery packs to power the engine. Voltage stabilization of insulated battery modules with the use of MLI is an important issue to consider. This issue occurs when the battery is both charging and discharging. Since battery modules are insulators, traditional BMS cannot perform voltage balancing and equal current operation. Therefore, there is a need for a reliable BMS specific to the MLI used. This complexity in BMS makes control difficult and increases its cost.

In baseband operating applications such as power rectifiers, active power filters or flexible AC transmission systems, multiple power supplies can be created from a single power supply. The operating frequency of the transformer is in the range of 20-50kHz, the volume of the transformer and capacitor has been reduced and is suitable for electric vehicles. These transformers isolate the input and output galvanically and adjust the voltage ratio according to the number of windings. Creating any voltage source using HFL requires the use of bridge diodes and capacitors. In fact, it does not require any control when creating an isolated voltage source, so it is widely used (Reimers et al., 2019). In addition, since the input voltage of all voltage busbars has a coefficient according to the number of turns, the input voltage changes proportionally to inverter output voltage.

In this study, the bypass diode MLI topology, which currently uses fewer switching elements compared to the recently published topologies, is implemented with a single DC source. In addition, the MLI is arranged asymmetrically to reduce the number of DC voltage units, switches, bridge diodes and capacitors. The NLC method is used to generate the output waveform with a low switching frequency. By taking the physical outputs of the HFL and the necessary circuits, NLC signals were produced with the Genesys 2 FPGA development board.

In the following sections, the studies are presented, the proposed topology circuit and working principle are explained, the findings obtained from the

simulation and experimental studies on this topology are presented, and the advantages of the proposed topology are given.

OPERATION CHARACTERISTICS

AC motors are increasingly used in EVs for performance and efficiency. Additionally, using a single voltage bus reduces the complexity of EV battery charging. Therefore, a topology with multilevel voltage waveforms at the output of a single DC power supply is proposed. The main structure and basic units of the proposed topology are shown in Figure 1.

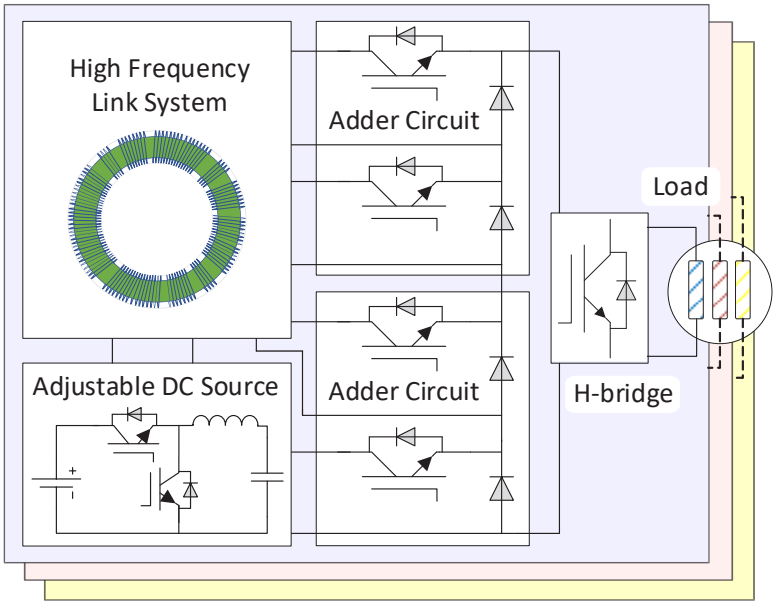


Figure 1: Proposed MLI topology

As shown in Figure 1, high frequency transformer is used to obtain an asymmetric DC-link voltage from a single DC source. The asymmetric DC level obtained using the HFL creates a multilevel output using a bypass diode circuit and an H-bridge.

The bus voltages of a single DC power supply are asymmetrically scaled (2^N) to achieve four different levels. 3 different DC bus voltages (1V:2V:4V) and 8V ratio mains supply voltage generated in 2^N operation using HFL are converted to multiple output for bypass diode circuits. The proposed topology can generate 15 positive voltages. The DC bus voltage will be as shown in Equation 1.

$$V_{Bus} = [S_0 S_1 S_2 S_3]_2 \cdot V_{DC} \quad (1)$$

1.1. High Frequency Link Circuit

The high frequency coupling circuit (HFL) generates high frequency AC signals applied from the secondary to the primary of the transformer according to the turn ratio. After rectification, isolated multiple DC voltage sources are obtained. This allows efficient power transfer while providing isolation between the two voltage sources. No control is required when using bridge diodes to create an auxiliary voltage (AUX) unit in the HFL circuit, as shown in Figure 2.

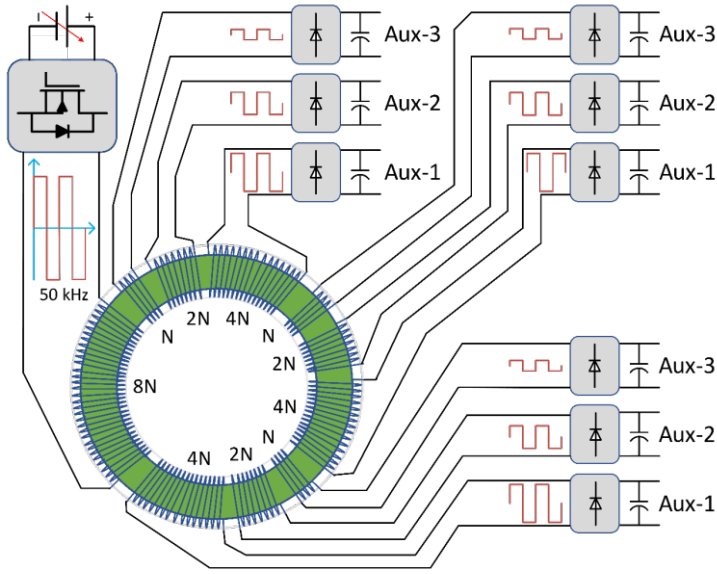


Figure 2: Proposed HFL topology

The H-bridge used here transmits less than half the power to the load and generates a high frequency square wave signal. It is used to reduce the size of high frequency transformers. A multi-winding toroidal transformer produces square wave signals with an amplitude of 2^N that are rectified by a simple bridge rectifier made of fast recovery diodes. The square wave signal produced by the HFL transformer is rectified by a bridge diode circuit.

1.2. Nearest Level Control

The nearest level control in the MLI is to trigger the power switch to keep the drive output voltage close to the reference outputs of the input. NLC has the advantages of fundamental switching frequency. Through this control strategy, the output of its limits can achieve high quality waves with less harmonics and

excellent dynamic performance. NLC is the height of the voltage closest to the reference voltage, as shown in Figure 3.

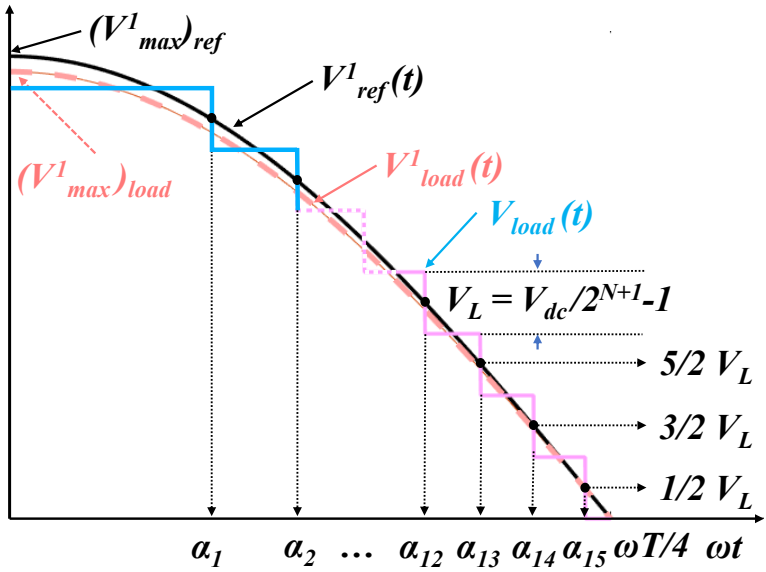


Figure 3: NLC controlled switching angle of the proposed topology

In Figure 3, the reference signal is taken as half of the step range. Half of the step-equal range of the resulting step signal always cuts off the reference signal. For example, for a positive 15-step output, generate the reference signal as a cosine with an amplitude of 15.5 units. The switching angle of the NLC is calculated according to the formula in Equation 2.

$$\alpha_i = \cos^{-1}\left(\frac{2^{N+2}-1-2i}{2^{N+2}-1}\right) \tag{2}$$

where i = 1, 2, …, 2N-1 and where N is the number of AUX units.

FPGA Signals

Xilinx System Generator (XSG) has integrated the FPGA with the Matlab program that engineers are prone to. In power electronics, control is usually provided by microcontrollers and DSPs (Zabun M. and Sedef H. 2021). XSG has been an effective method for rapidly prototyping, testing and developing hardware without the need for HDL knowledge. The operation can be evaluated using XSG without loading the signals generated by using Matlab/Simulink

blocks to the FPGA board. After the necessary arrangements, the VHDL code is automatically generated and programmed into the FPGA (Selvamuthukumaran and Gupta, 2014).

In order to sum the four different voltages in the bypass diode circuit, it is necessary to have four separate signals. The binary number is represented by the number $S_0S_1S_2S_3$, depending on what time interval the signals will be provided at each level. As shown in Figure 4, it summarizes the process of obtaining these signals by the NLC method.

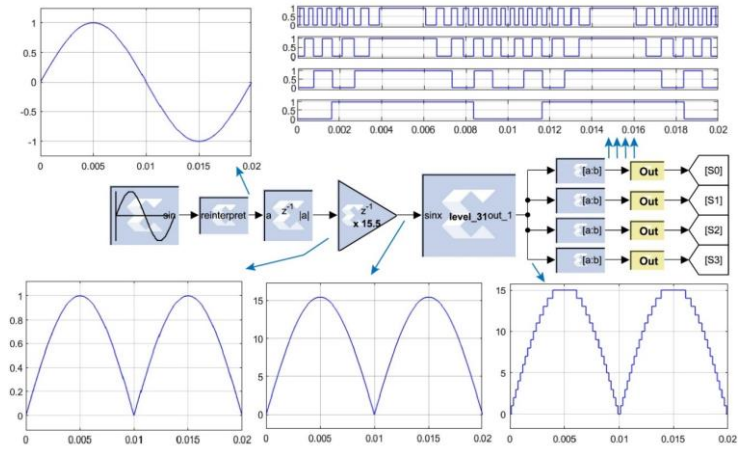


Figure 4: Supply of $S_0S_1S_2S_3$ NLC signals

SIMULATION RESULTS

When a 100V square signal is applied to the transformer input, the square signals formed at the output for 1 phase are shown in Figure 5.

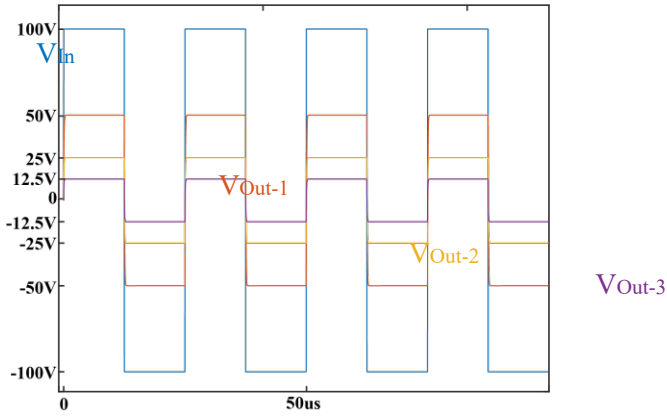
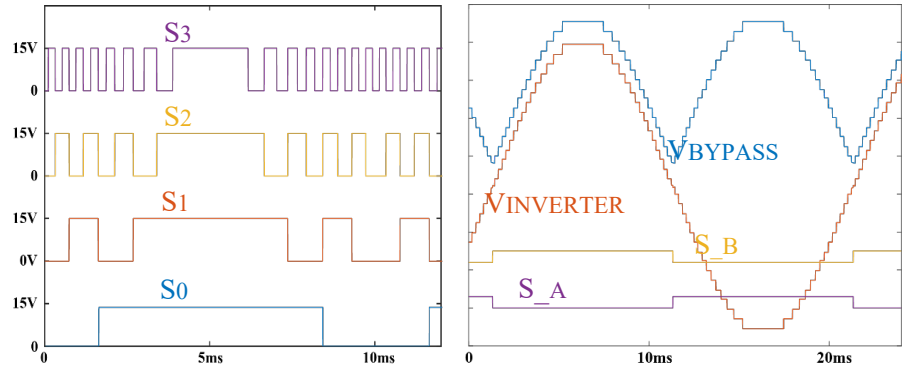


Figure 5: When a 100V square signal is applied to the transformer input, square signals are formed at the output for 1 phase.

As seen in Figure 5, when a 100V square wave signal is applied to the transformer input, square wave signals with amplitudes of 50V, 25V and 12.5V will be obtained at the output, respectively, depending on the conversion ratio.

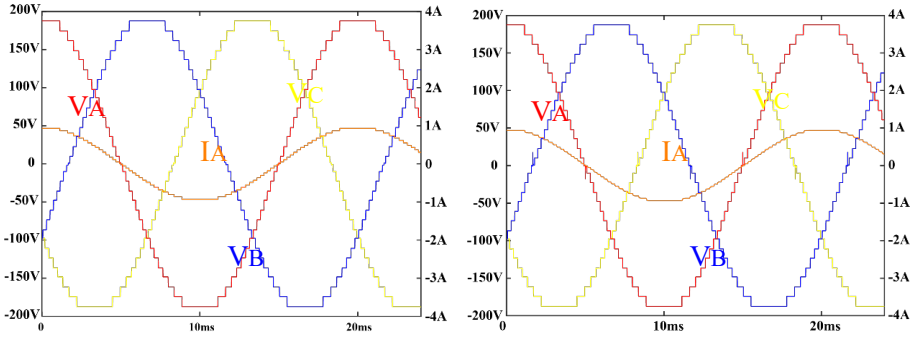
The switching signals applied to the bypass diode circuit by the NLC are shown in Figure 6a, and the bypass diode circuit output, the inverter output and H-bridge signals are shown in Figure 6b.



(a) (b)

Figure 6: (a) Switching signals, (b) Bypass diode circuit output, the inverter output, H-bridge signals.

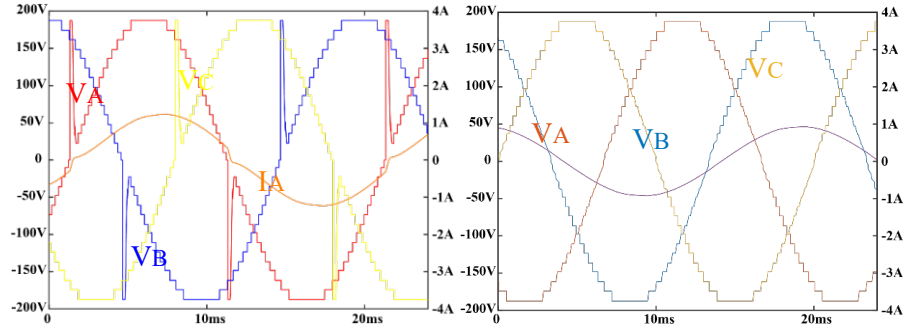
A 150ohm resistor is used in the simulation environment. The inverter phase voltages and phase current of the case of pure resistive load with collector switch signals are given in Figure 7a. The inverter phase voltages and phase current formed by the effect of inductive filter on pure resistive load are given in Figure 7b.



(a) (b)

Figure 7: The inverter phase voltages and phase current (a) Pure resistive load (b) Inductive filter effect

The phase voltage and phase current of the induction motor model are shown in Figure 8a without using any filter to the output of the proposed MLI topology and are obtained using a 5uF capacitive filter to the motor terminal. Voltage and current with capacitive filter are shown in Figure 8b.



(a) (b)

Figure 8: Induction motor phase voltages and phase current (a) when no filter is used, (b) when capacitive filter is used

It can be seen from Figure 8a that there is a jump at the zero crossing of the phase voltage obtained by the NLC control method and there is a slight jump in the current due to the voltage jump. A 5uF capacitive filter parallel to the motor terminals eliminates zero-crossing as shown in Figure 8b. Also, improving the phase voltage improves the signal quality by correcting the phase current.

EXPERIMENTAL RESULTS

The experimental setup of the 3-phase 31-level MLI topology circuit proposed in the study is given in Figure 9. A 150ohm resistor is used in the experimental setup.

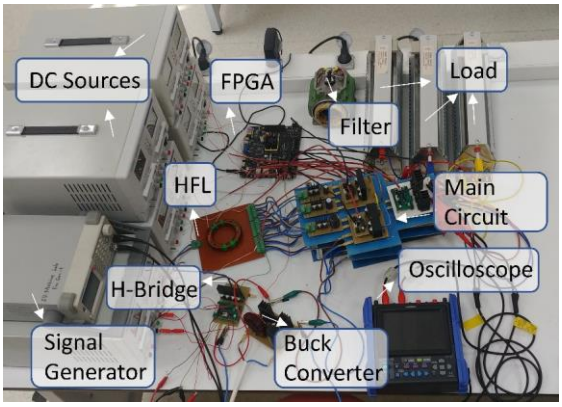
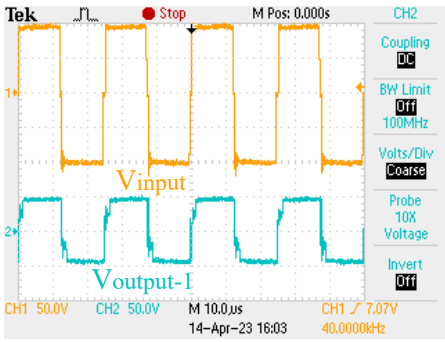


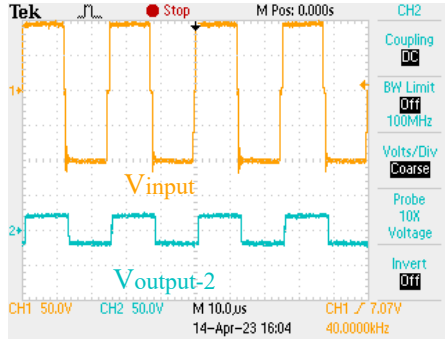
Figure 9: Experimental setup of the proposed topology

The H-bridge takes the voltage from a single DC source in Figure 9 and generates a square wave signal there. A multi-output toroidal transformer rectifies this square wave signal by multiplying different voltages. The bypass diode circuit then collects this signal according to the NLC method. The output of this process converts it into a sinusoidal form, positive and negative, with another H-bridge before being transmitted to the load.

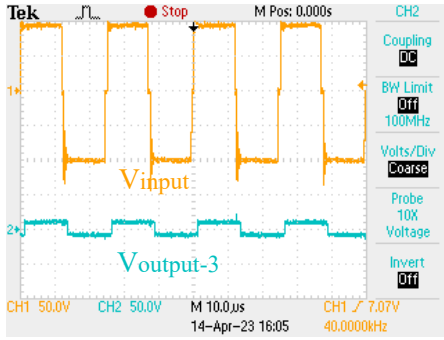
Figure 10 shows the square wave signal generated at the output of the transformer when a 100V square wave signal is applied to its input. The generated square signals were obtained according to single phase.



(a)



(b)

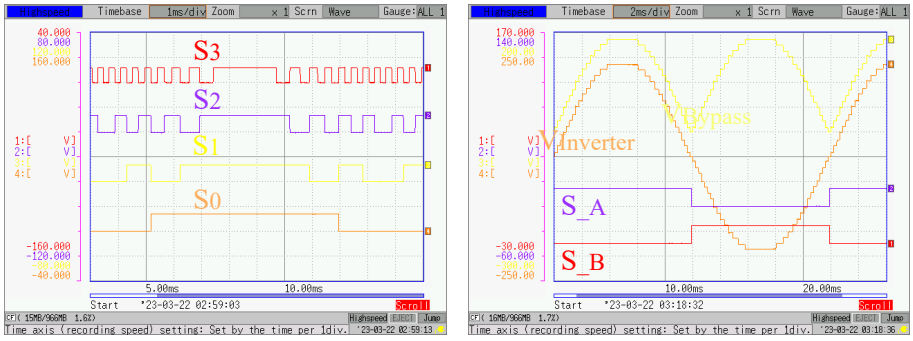


(c)

Figure 10: Toroid transformer: (a) Primary voltage and first output voltage (b) Primary voltage and second output voltage (c) Primary voltage and third output voltage

As seen in Figure 10, when a 100V square signal is applied to the transformer input, square signals with 50V, 25V and 12.5V amplitudes are obtained at the output, depending on transformer conversion ratios, respectively.

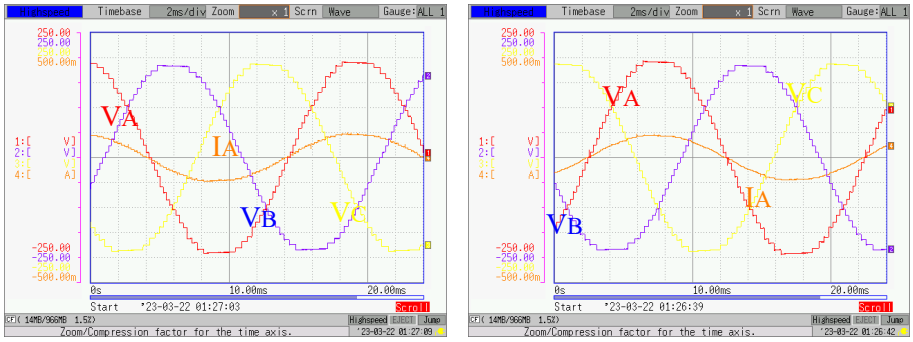
The switching signals generated from the bypass diode driver circuit and the bypass diode circuit output, inverter output, H-bridge driver signals are given in Figure 11a and Figure 11b, respectively.



(a) (b)

Figure 11: Bypass diode circuit (a) switching signals generated from the driver (b) Bypass diode circuit output, the inverter output, H-bridge driver signals

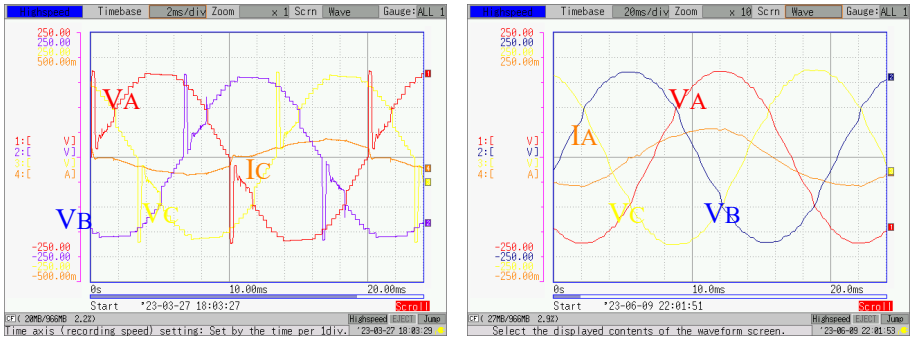
The inverter phase voltages and phase current of the bypass diode switch signals, when the load is pure resistive, are shown in Figure 12a and the phase voltages and phase current obtained by using an inductive filter are shown in Figure 12b.



(a) (b)

Figure 12: The inverter phase voltages and phase current (a) at pure resistive load (b) with inductive filter

The phase voltages and phase current obtained when the induction motor is connected to the output of the MLI topology without using any filters are shown in Figure 13a. The motor terminal voltages and current obtained using a 5uF capacitor filter are shown in Figure 13b.



(a) (b)

Figure 13: Induction motor phase voltages and phase current: (a) when no filter is used, (b) when capacitive filter is used

As seen in Figure 13a, there is a jump at the zero-crossing of the phase voltage, and a slight jump in current due to the voltage jump. A 5uF capacitive filter parallel to the motor terminals eliminates zero-crossing transitions as shown in Figure 13b. Also, improving the phase voltage improves the signal quality by correcting the phase current.

RESULTS AND DISCUSSION

The main advantage of the asymmetric multilevel inverter is to achieve the maximum output level with the minimum number of power supplies. Numerous isolated DC sources complicate the battery and charging system. The HFL used in this study reduces the multiple DC power supplies required by the main topology to a single power supply, allowing it to be applied to EV. Advantages and disadvantages of the proposed topology and possible solutions to these disadvantages are given.

When determining the type of EV driver, it is expected that the cost, complexity, size and weight of the drive system will be reduced in such a way as to make the greatest contribution to the vehicle. Cost is budgeted for by the end user, complexity is difficult to control, reduction in volume leads to more room in the vehicle for other components, and weight leads to a reduction in the overall weight of the vehicle.

Recently, EV manufacturers have tended to increase battery voltage. The use of MLI in high-power and high-voltage applications for electric ships and electric trains coincides with the usability of these topologies in electric vehicles. If an 800V battery that supports fast charging is used, a motor designed for 1500V can be connected to the inverter output. In fact, the proposed topology can operate at high voltages with low-voltage switches, thus

reducing switching costs. It reduces the cost, size and weight of motors and wiring.

The fact that the HFL system accounts for 45% of the total power reduces the load on the switches directly connected to the bypass diode circuit of the power supply. Choosing these low voltage switches can reduce cost. Since the square wave signal is rectified in the rectification circuit and the capacitors used do not reduce the current from the motor, they are chosen with low capacitance. This reduces volume and cost.

Overuse of switches and drivers in MLI adds cost and complexity. Having fewer switches compared to other MLI topologies is advantageous in terms of number of switch drivers and cooler volume. Since boards such as FPGA and DSP generate switching signals in direct control mode, complexity is reduced to controlling a single switch.

When the inverter output voltage exceeds zero, there will be a voltage spike due to the main topology. This jump is avoided by parallel filtering with low value non-polarized capacitors. When the engine is running at low speed, the zero-cross voltage jump also blocks the capacitor used, causing the engine to hit the cylinder. However, due to the relatively low THD, this knock is not as strong as with conventional inverters. Because the zero-cross voltage form of the proposed topology is higher quality than the low-speed conventional inverter.

The high frequency operation of the transformer and HFL H-bridge circuit used in the proposed topology reduces the overall efficiency. Using a solid-state transformer instead of a toroidal transformer can improve overall efficiency. Additionally, replacing HFL H-bridge switches with switches with low internal resistance and short rise and fall times, such as GaN or SiC, can improve overall efficiency.

CONCLUSION

In this study, a 31-stage MLI circuit is implemented using a small HFL-based asymmetric adder with a single DC source with fewer switching elements than recently published topologies. It has been observed that the use of a low-value inductance filter makes the current form highly sinusoidal, while a high-inductance filter causes zero-crossing voltage transitions. At the proposed MLI output, a zero-voltage crossover jump is observed due to the high inductive load when using an AC motor. It is seen that this jump voltage can be eliminated with a small capacitor connected parallel to the output of the proposed topology. According to simulation and experimental research, the THD value of the 31-

stage output voltage of the NLC method is below 5%, meeting IEEE 519 and TS-EN50160 standards.

It has many advantages over similar studies using MLI circuits. The outstanding value of this study is that compared to the output level of this study, less switches are used in other topologies and the number of switching is less, which reduces the control load of the system and increases reliability. In addition, the use of fewer capacitors in the proposed topology, significantly lower THD than conventional inverters, low voltage change ratio and low EMI indicate the importance of this research. The proposed topology has the advantages of having fewer switches than other MLI topologies, in terms of the number of key drivers and heatsink volume.

The use of lower switching elements reduces switching losses and the cost of the proposed topology. Also, AUX units can be chosen as their capacitors are relatively small as they only absorb energy from the load for a short time in the regenerative braking situation. Using one H-bridge per phase in the circuit and operating it at the fundamental frequency increases the efficiency of inverter. Since it can be powered by a single battery, it can be used in electric vehicle inverter applications and other industrial applications that require multiple isolated DC power supplies. In the proposed topology, the power switches operate at the fundamental frequency. A reference signal frequency proportional to motor speed reduces power loss and cooler requirements. It also helps to use motor control systems such as voltage/frequency where control is done with the reference signal frequency and frequency variation is important.

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